

What is claimed is:

1.           A data output circuit which outputs data on an  
2 internal bus line onto an external bus line, comprising:  
3           comparison means for comparing data on the  
4 external bus line and data to be output on the internal  
5 bus line;  
6           inversion means for outputting a signal  
7 obtained by inverting the data on the internal bus line  
8 when the number of changed bits exceeds half the total  
9 number of bits on the basis of an output result from  
10 said comparison means; and  
11           control means for outputting an inversion  
12 display signal representing that the data has been  
13 inverted.

2.           A circuit according to claim 1, wherein said  
2 comparison means, said inversion means, and said control  
3 means constitute an output data control unit.

3.           A circuit according to claim 2, further  
2 comprising:  
3           an amplifier which amplifies read data;  
4           data latch means for latching data output from  
5 said amplifier; and  
6           input/output means for transmitting an output  
7 data bus signal from said output data control unit as

8 output data onto the external data bus.

4. A circuit according to claim 3, wherein said  
2 input/output means feeds back the output data to said  
3 comparison means.

5. A circuit according to claim 3, further  
2 comprising clock signal supply means for supplying a  
3 clock signal to said data latch means, said output data  
4 control unit, and said input/output means.

6. A circuit according to claim 1, wherein the  
2 data on the internal bus line includes data read out  
3 from storage means.

7. A circuit according to claim 1, wherein said  
2 comparison means and said control means are arranged for  
3 each of groups obtained by classifying internal bus  
4 lines into a plurality of groups.

8. A data output method of outputting data on an  
2 internal bus line onto an external bus line, comprising  
3 the steps of:

4 comparing data on the external bus line and  
5 data to be output on the internal bus line;

6 when the number of changed bits exceeds half  
7 the total number of bits on the basis of a comparison

8 result, inverting the data on the internal bus line to  
9 output the data onto the external bus line; and  
10 outputting a data inversion signal  
11 representing that the data has been inverted.

9. A method according to claim 8, wherein the  
2 comparison step comprises the step of receiving a clock  
3 signal.

10. A method according to claim 8, further  
2 comprising the step of reading out the data on the  
3 internal bus line from storage means.

11. A method according to claim 8, wherein  
2 the comparison step comprises the step of  
3 performing the comparison step for each of groups  
4 obtained by classifying internal bus lines into a  
5 plurality of groups, and  
6 the output step comprises the step of  
7 performing the output step for each of the groups  
8 obtained by classifying the internal bus lines into the  
9 plurality of groups.